I CLAIM:

1. An apparatus comprising:

a clock encoding circuit configured to receive a source clock signal, wherein said clock encoding circuit is configured to generate an encoded system clock signal using said source clock signal;

a clock decoding circuit configured to receive said encoded system clock signal, wherein said clock decoding circuit is configured to generate a phase signal and a core clock signal using said encoded source clock signal; and

a clock generating circuit configured to generate a global clock signal using said phase signal and said core clock signal, and wherein said clock generating circuit is configured to generate a system clock signal that is synchronous with said global clock signal using said encoded clock signal.

2. The apparatus of claim 1, wherein said encoded system clock includes a first plurality of pulses and a second plurality of pulses, and wherein said first plurality of pulses correspond to a different duty cycle than said second plurality of pulses.

3. The apparatus of claim 2, wherein said first plurality of pulses correspond to a longer duty cycle than said second plurality of pulses.

4. The apparatus of claim 2, wherein said first plurality of pulses correspond to a shorter duty cycle than said second plurality of pulses.

5. The apparatus of claim 2, wherein each of said first plurality of pulses occurs at a regular interval of said encoded system clock.

6. The apparatus of claim 2, wherein each of said first plurality of pulses is followed by an integer number of said second plurality of pulses, and wherein said integer number is greater than one.

7. The apparatus of claim 2, wherein said encoded system clock includes a third plurality of pulses, wherein said third plurality of pulses correspond to a same duty cycle as said first plurality of pulses, and wherein said third plurality of pulses include encoded information.

8. The apparatus of claim 2, wherein said pulse signal includes a third plurality of pulses, wherein said third plurality of pulses correspond to said first plurality of pulses.

9. A method comprising:

generating an encoded clock signal using a source clock signal;

generating a pulse signal and a core clock signal using said encoded clock signal;

generating a global clock signal using said pulse signal and said core clock; and

generating a system clock signal that is synchronous with said global clock signal using said encoded system clock.

10. The method of claim 9, wherein said generating said encoded clock signal includes:

generating a first plurality of pulses; and

generating a second plurality of pulses;

wherein said first plurality of pulses correspond to a different duty cycle than said second plurality of pulses.

11. The method of claim 10, wherein said first plurality of pulses correspond to a longer duty cycle than said second plurality of pulses.

12. The method of claim 10, wherein said first plurality of pulses correspond to a shorter duty cycle than said second plurality of pulses.

13. The method of claim 10, wherein each of said first plurality of pulses is followed by an integer number of said second plurality of pulses, and wherein said integer number is greater than one.

14. The method of claim 10, wherein said generating said encoded clock signal includes:

generating a third plurality of pulses, wherein said third plurality of pulses correspond to a same duty cycle as said first plurality of pulses, and wherein said third plurality of pulses include encoded information.

15. An apparatus comprising:

a clock encoding circuit configured to receive a source clock signal, and wherein said clock encoding circuit is configured to generate an encoded clock signal using said source clock signal; and

a plurality of devices coupled to said clock encoding circuit, wherein each of said plurality of devices includes:

a clock decoding circuit configured to receive said encoded system clock signal, wherein said clock decoding circuit is configured to generate a phase signal and a core clock signal using said encoded source clock signal; and

a clock generating circuit configured to generate a global clock signal using said phase signal and said core clock signal, and wherein said clock generating circuit is configured to generate a system clock signal that is synchronous with said global clock signal using said encoded clock signal.

16. The apparatus of claim 15, wherein said encoded system clock includes a first plurality of pulses and a second plurality of pulses, and wherein said first plurality of pulses correspond to a different duty cycle than said second plurality of pulses.

17. The apparatus of claim 16, wherein said first plurality of pulses correspond to a longer duty cycle than said second plurality of pulses.

18. The apparatus of claim 16, wherein said first plurality of pulses correspond to a shorter duty cycle than said second plurality of pulses.

19. The apparatus of claim 16, wherein each of said first plurality of pulses occurs at a regular interval of said encoded system clock.

20. The apparatus of claim 16, wherein each of said first plurality of pulses is followed by an integer number of said second plurality of pulses, and wherein said integer number is greater than one.

21. The apparatus of claim 16, wherein said encoded system clock includes a third plurality of pulses, wherein said third plurality of pulses correspond to a same duty cycle as said first plurality of pulses, and wherein said third plurality of pulses include encoded information.

22. The apparatus of claim 16, wherein said pulse signal includes a third plurality of pulses, wherein said third plurality of pulses correspond to said first plurality of pulses.